ASIC Flow

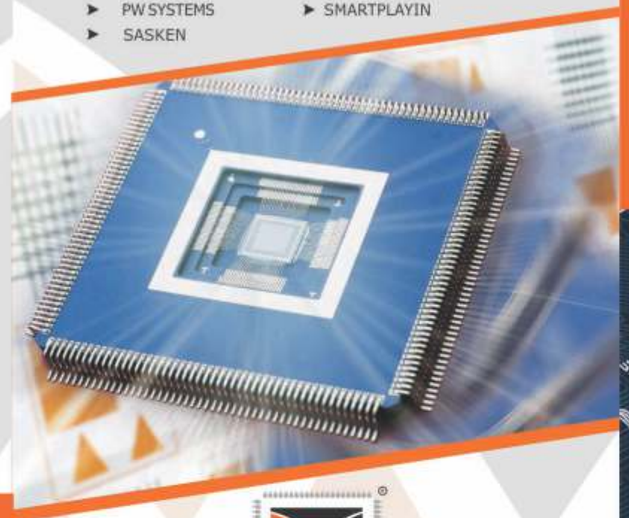
- EDA Tools/CAD Flow for IC Design
- Simulation/Synthesis using ASIC libraries
- Clock tree synthesis
- False paths / Multi cycle paths/Critical paths
- Design for testability (DFT)
- Scan Insertion/Types of scan
- Fault models
- Logic BIST, Memory BIST, ATGP, Boundary Scan
- Pattern Compression
- Scan Diagnostics
- Layout Design
- Placing and Routing
- LVS/DRC/OPC/Physical verification
- Diagnosis, DFM, Yield analysis
- SOC Design and Trade-offs
- Future trends and Challenges
- ASIC Case Studies

Companies Hiring Embedded Students

Ikanos Communication, Global Edge Software, Intense Technologies, GD Micro, Schnider Electric, ELICO, Fortuna Technologies, Intoto, Dear Born Electronics, HSBC GTC, Knowx Innovation, Huawei Technologies, E-Con Systems, General Motors, Safran Aerospace, Mistral Solutions, Ordyn Communication, Cavium Networks, TINS, Siemens, Transcon Industries, Wineyard Technologies, Delphi, Convergys, Crompton Greaves India Pvt Ltd, Blue Chip, Sasken Communications, VenSoft, Mars Telecom, TietoEnator, Vedams, Philips, Pandora Networks, Azingo(Celunite), VEM Technologies, Infosys, Inside Mobile, Megasoft, Cyber Motions India Pvt Ltd, VXL, Robert Bosch, Saha, Software Sol, Visteon, EmSyS, 3COM, Lear Corporation, Transvalves, EA-Mobile, LGSoft, Ceeyes, Sankhya Technologies, Park Controls & Communications, Midas Communications, ESSEN Electronics, Satyam, Conexant, Panterra Networks, Tata Power-SED, Moschip Semiconductors, Aricent, Key-point Technologies, Aizyc (Embd & VLSI), Fusion Networks, Touchmeme, Emerson Network Power, Nomus Comm Systems, NX Bio, Polycom R&D, Neucleonix Sys, Linkwell Telesystems, Gaian Solutions, Infotech, Team F1, SQL Star, Nokia Siemens, Bartronics, Srans Info System, Automotive Robotics, American Meghatrends Inc, KPT, Cadence, Synfosys, Prime Soft, Grit Innvations, Apollo Micro Systems, Vayguru Systems, Danlaw Inc, Latens Systems, Samsung, Hellosoft, Winit, MCN Technologies, Latens, Systems, Powai Labs (VLSI), Seven Technologies, Fat Pipe Networks, Sparsh Comm, Purple Talk, Copper Head Sys, Rock Well Collins, Msys Tech, Votary Tech, Persistent, GoDB Systems, Qteq Info Solutions, Pentagon Systems, Microgenisis Technologies and many more ...

Companies Hiring VLSI Students

- CADENCE
- APOLLO MICRO SYS
- POWAI LABS
- PW SYSTEMS
- SASKEN
- PERFECTUS TECHNOLOGIES
- NV LOGICS
- HELLOSOFT
- SMARTPLAYIN



VECTOR INSTITUTE

Drives you to Industry

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ASIC/FPGA DESIGN

ISO 9001:2008 CERTIFIED INSTITUTE

Tools For FPGA

Simulation	:	Modelsim, Questa
Systhesys	:	Precision RTL, Leonardo Spectrum, Synplify
Place and route	:	Xilinx ISE, Altera Quartus

Tools For ASIC

Simulation	:	Modelsim, Questa
Synthesys	:	Design Compiler
Place & Route	:	IC-Station
STA	:	Primetime
ATPG/EDT	:	TestKompress

Other Tools

MBIST Architect, LBIST, BSD Architect (JTAG)
Physical Verification/DRC/LVS : Calibre suite

www.vectorindia.org

About Us

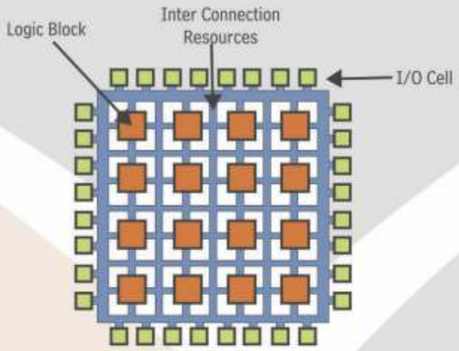
- Vector Software Professional Training Institute established with an objective to train students & drive them to industry.
- Directors with over a decade of rich industry experience in Design, Development, Training and Recruitment.
- Directors have worked with fortune 500 companies like Damlier Chrysler, General Motors, Ford and also with scientific organizations like DRDL, involved in the development of high precision products, using cutting edge technologies.
- Supported by Industry experts from technical & H.R. Departments.
- Vector's experienced faculty brings real time exposure and experience to the Classroom.

Course Objective

- These programs are specifically designed with an objective to create quality manpower in the fields of VLSI Design, VLSI System Design with FPGA's and ASIC's, imparting quality hands-on training from 'concept-to-project', covering design methodology using industry standard tool and practices.
- All faculties are from our Vector Team and they share their industry knowledge on Design Concepts, Coding, Best and Most effective way of usage of EDA Tools. This makes significant difference to the program and also to the quality of Engineers Graduating from the institute.
  - Faculty consisting of industry experts with wide practical exposure
  - Best design practices offered on industry standard EDA tools
  - State-of-the-art infrastructure
  - Extensive hands-on sessions on NT and SUN Platform
- The Program is delivered in a teacher directed, student centered setting. This structured environment maximizes teaching and learning and fosters both personal freedom and responsibility.
- We offer a wide range of courses in VHDL, Verilog, Verification, ASIC design, FPGA design and Tool Specific training.

ASIC/FPGA DESIGN

- ASIC /FPGA Design Fundamentals
- Advanced Digital Design



CMOS

- MOS Fundamentals and Characterization
- NMOS / PMOS / CMOS Technologies
- Fabrication Principles
- Different Styles of Fabrication for NMOS / PMOS / CMOS
- Design with CMOS Gates
- Characterization of CMOS Circuits
- Scaling Effects
- Sub-Micron Designs
- Parasitic Extraction and Calculations
- Subsystem Design
- Layout Representation for CMOS Circuits
- Design Exercise using CMOS
- Introduction of IC Design
- Different Methodologies for IC Design
- Fabrication Flows and Fundamentals

Admission through All India Entrance Test

HARDWARE DESCRIPTION LANGUAGES

VHDL

- Vhdl overview and concepts
- Levels of abstraction
- Entity, Architecture
- Data types and declaration
- Enumerated data types
- Relational, Logical, arithmetic operators
- Signal and variables, constants
- Process statement
- Concurrent statements
  --When-else, with-select
- Sequential statement
  --if-then-else, Case
- Slicing and Concatenation
- Loop Statements
- Delta delay concept
- Arrays, Memory modeling, FSM
- Writing procedures
- Writing functions
- Behavioral/RTL coding
- Operator overloading
- Structural coding
  --Component declarations and instantiations
- Generate statement
- Configuration block
- Libraries, Standard packages
- Local and global declarations
- Package, Package body
- Writing test benchs
- Assertion based verification
- File read and write operations
- Code for complex FPGA and ASICs
- Generics and Generic maps

Internal Assessment, Mock Interviews, Personality Development Classes

VERILOG

- Language introduction
- Levels of abstraction
- Module, Ports types and declaration
- Registers and nets, Arrays
- Identifiers, Parameters
- Relational, Arithmetic, Logical, Bit-wise shift operators
- Writing expressions
- Behavioral modeling
- Structural coding
- Continuous assignments
- Procedural statements
  --Always, Initial blocks
  --begin ebd, fork join
- Blocking and Non-blocking statements
- Operation control statements
  --if, case
- Loopswhile, for-loop, foreach, repeat
- Combination and sequential circuit designs
- Memory modeling, state machines
- CMOS gate modeling
- Writing tasks
- Writing functions
- Compiler directives
- Conditional compilation
- System tasks
- Gate level primitives
- User Defined Primitives
- Delays, Specify block
- Testbenchs, Modeling, Timing checks
- Assertion based verification
- Code for synthesis
- Advanced Topics
- Writing reusable code

Highly Application Oriented Training

SYSTEM VERILOG

- Introduction to System Verilog
- System verilog Declaration Spaces
- System Verilog Literal Values and Built-in Data Types
- System Verilog User-Defined and Enumerated Types
- System Verilog Arrays, Structures and Unions
- System Verilog Procedural Blocks, Tasks and Function
- System Verilog Procedural Statements
- Modeling Finite State Machines with System Verilog
- System Verilog Design Hierarchy
- System Verilog Interfaces
- Behavioral and Transaction Level Modeling

FPGA Flow

- Re-configurable Devices, FPGA's/CPLD's
- Architectures of XILINX, ALTERA devices
- Designing with FPGAs
- FPGA's and its Design Flows
- Architecture based coding
- Efficient resource utilization
- Constraints based synthesis
- False paths and multi cycle paths
- UCF file creation
- Timing analysis/Floor Planning
- Place and route/RPM
- Back annotation, Gate level simulation, SDF Format
- DSP on FPGA
- Writing scripts
- Hands on experience with Industry standard tools.